

PARALLEL PROGRAMMING AND OPTIMIZATION TRAINING INTEL® XEON PHI™ COPROCESSORS

This professional training is designed for programmers who are looking to develop skills in application design and optimization for Intel Xeon Phi coprocessors.

Participants will be provided with an introduction to available programming models, the tools and the knowledge needed to accelerate highly-parallel algorithms by taking advantage of the Intel Many Integrated Core (Intel MIC) Architecture.

Learn from the best

The training material has been established in collaboration with Intel and includes commercial optimization techniques developed by Acceleware. Established in 2004 Acceleware has been developing high performance applications for almost a decade!

The courses are taught by Acceleware programmers who bring real world experience into the classroom. To date Acceleware has delivered over 100 courses across four continents, teaching hundreds of programmers how to design high performance applications.

Key outcomes

A combination of lectures, case studies and hands-on exercises will provide participants with an understanding of:

- Intel Xeon Phi coprocessor architecture
- Available execution models including offloading and native execution
- Memory models including using pragmas and virtual-shared memory
- Debugging and profiling tools
- Optimization techniques for both memory bandwidth and compute bound algorithms

Course features

- Small class sizes to maximize learning
- Hands-on exercises developed by our experts
- Individual laptops for student use
- Printed manual of all lectures
- Electronic copy of lab exercises
- Certificate of completion

Contact services@acceleware.com to find out more about our Xeon Phi training.

Course outline

Introduction

- Overview of Xeon Phi coprocessor
- Xeon Phi coprocessor programming model

Using OpenMP with the Xeon Phi coprocessor

- Introduction to OpenMP
- Work sharing and race conditions in OpenMP
- Profiling
- Scheduling and data clauses
- OpenMP runtime library and environment variables
- Hands-on exercises: Launching a multi-threaded application, arithmetic reduction, using VTune, matrix multiply, environment variables and runtime libraries

Using MPI with the Xeon Phi coprocessor

- Introduction to MPI
- MPI communications
- OpenMP & MPI
- Hands-on exercises: Launching an MPI enabled application, scatter and gather exercise, OpenMP and MPI

Optimization

- Introduction to Xeon Phi architecture and optimization
- Vectorization
- Memory optimizations
- Hands-on exercise: Choosing the number of hardware threads, vectorization with pragmas and by hand and memory optimizations

Tools & Installation

- Debugging
- Intel MKL libraries
- System configuration
- Hands-on exercise: Debugging, MKL library

