"The OpenCL introduction, lectures, and exercises were excellent, as well as the application to FPGAs, which was the most useful to me."

Vincent Pierre
Toshiba Medical Research Institute USA, Inc.

Learn from the Experts
OpenCL for Intel FPGAs

acceleware

This professional 4 day course focuses on how to write and optimize OpenCL applications for Intel FPGAs. Students will be taught how to achieve high performance by taking advantage of the heterogeneous nature of OpenCL and the massively parallel capabilities of Intel FPGAs. The training is targeted at design teams who work with parallel algorithms and computationally intense applications.

LEARN FROM THE BEST

The courses are taught by Acceleware programmers who bring real world experience into the classroom. To date Acceleware has delivered over 100 courses across four continents, teaching hundreds of programmers how to run computations faster with OpenCL training.

HANDS-ON EXERCISES

In addition to the published class schedule Acceleware offers private on-site courses. We will travel to your location and can tailor the content specifically to your needs.

KEY OUTCOMES

This couse is designed to accelerate your development efforts by 4-6 months. Key learning objectives include:

- Mastering the basics of OpenCL
- Using local and constant memory to improve performance
- Taking advantage of all system resources in parallel
- Debugging OpenCL programs and numerical accuracy
- Targeting Intel FPGAs with OpenCL
- Compililng OpenCL kernels to Intel FPGAs
- Optimizing Intel FPGA kernels for throughput and size trade-offs
- Using efficient memory access patterns and Intel OpenCL attributes to optimize memory performance

Course Outline

Day 1:

- Introduction to OpenCL
- Overview of OpenCL software
- Hands-on-Exercise (x2)
- Data-parallel architectures and the OpenCL programming model

Day 2:

- OpenCL memory model and work item cooperation
- Hands-on-Exercise (x3)
- OpenCL task concurrency and synchronization
- Debugging OpenCL programs and numerical accuracy

Day 3:

- Compiling OpenCL kernels to Intel FPGAs
- Hands-on-Exercise (x3)
- Throughput and size trade-offs
- Memory optimizations

Day 4:

- Case study
- OpenCL architectures: compare and contrast
- Hands-on-Exercise

Wrap-up

www.acceleware.com training@acceleware.com 1.403.249.9099