

Professional Training for Intel Xeon Phi Coprocessors



This professional training course is designed for programmers who are looking to develop skills in application design and optimization for Intel Xeon Phi coprocessors.

Participants will be provided with an introduction to available programming models, the tools and the knowledge needed to accelerate highly-parallel algorithms by taking advantage of the Intel Many Integrated Core (Intel MIC) Architecture.

LEARN FROM THE BEST

The training material has been established in collaboration with Intel and includes commercial optimization techniques developed by Acceleware. The courses are taught by professionals who bring real world experience into the classroom. To date Acceleware has delivered over 100 courses across four continents, teaching hundreds of programmers how to design high performance applications.

KEY OUTCOMES

A combination of lectures, case studies and hands-on exercises will provide participants with an understanding of:

- Intel Xeon Phi coprocessor architecture
- Available execution models including offloading and native execution
- Memory models including using pragmas and virtual-shared memory
- Debugging and profiling tools
- Optimization techniques for both memory bandwidth and compute bound algorithms

Course Outline

Introduction

- Overview of Xeon Phi coprocessor
- Xeon Phi coprocessor programming model

Using OpenMP with the Xeon Phi coprocessor

- Introduction to OpenMP
- Work sharing and race conditions in OpenMP
- Scheduling and data clauses
- OpenMP runtime library and environment variables
- Hands-on exercises

Using MPI with the Xeon Phi coprocessor

- Introduction to MPI
- MPI communications
- OpenMP & MPI
- Hands-on exercises

Optimization

- Introduction to Xeon Phi architecture and optimization
- Vectorization
- Memory optimizations
- Hands-on exercises

Tools & Installation

- Debugging
- Intel MKL libraries
- System configuration
- Hands-on exercise